Satyug Darshan Institute of Technology,Faridabad

	Programme: B.Tech -CSE	**Year:/Semester:2nd Year & 3rd Sem**
	Subject Name : Digital Electronics	**Subject Code: ELU-202-V**

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Unit -1

Short Questions

S. No.	Questions	Bloom Taxonomy
1	Write the gray code for (11100011)2.	KL2
2	Perform binary addition: 1011+1101.	KL3
3	List any one advantage of CMOS circuits over TTL circuits.	KL1
4	Convert (F4ED.3E)16 to ( )8.	KL3
5	(100011)2 – (110101)2 using 2s complement method.	KL3
6	Convert the following (18.53)10 to ( )16	KL3
7	Define the term 'Fan Out' of any digital IC.	KL1
8	Explain the concept of temporal code.	KL1
9	Discuss the advantages of CMOS families used for implementing logic gates.	KL2
10	Explain the implementation of a NAND gate using only NOR gates.	KL1

Long Questions

1	List the advantages of CMOS logic families used for implementing logic gates.	KL1
2	Describe error correction and detection codes.	KL2
3	Define the AND, OR, NOT, NAND, NOR and Exclusive-OR (XOR) operations. Provide the truth table for each.	KL2
4	Describe the internal structure of a TTL tristate gate and also drae the diagram.	KL2
5	Explain interface between TTL to CMOS circuit. Also write the necessity of interfacing in logic circuits.	KL2

Unit -2

Short Questions

S. No.	Questions	Bloom Taxonomy
1	Distinguish between demultiplexer and multiplexer.	KL2
2	Write the application of decoder.	KL2
3	Draw logic diagram of full adder.	KL1
4	Draw the truth table for half adder circuit.	KL1
5	Design 2-bit comparator and draw logic diagram.	KL3
6	Draw the truth table for 1-bit comparator circuit.	KL1
7	Explain the difference between an encoder and priority encoder.	KL2
8	Distinguish between arithmetic and logic operations in ALU.	KL2
9	Perform the BCD subtraction of (73)10 – (38)10	KL3
10	Differentiate between a prime implicant and an essential prime implicant.	KL2

Long Questions

S. No.	Questions	Bloom Taxonomy
1	Minimize the following function in SOP minimal form using K-Maps. f = m (1, 5, 6, 11, 12, 13, 14) + d (4)	KL3
2	Explain the function of a 4:1 multiplexer with a block diagram and truth table.	KL2
3	Describe the function full adder with a truth table and Boolean expressions for the sum and carry outputs. Draw a basic logic circuit diagram for a full adder.	KL2
4	Simplify the Boolean algebra function using tabulation method. $f(A,B,C,D) = \sum m(0,2,3,6,7,8,10,12,13)$	KL2
5	Minimize the given expression using K map and draw the diagram with NAND gate. $f(A,B,C,D) = \sum m(8,9,10,11,13,15,16,18,21,24,25,26,27,30,31)$	K3

6	Differentiate between serial carry and CLA with suitable diagram.	KL2
7	Reduce the following Boolean Algebra Expression: $f(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{C} + \overline{(A+B+C)} + \overline{A}\,\overline{B}\,\overline{C}\,D$	KL3
8	Implement function F (A, B, C) = Σ (1,3,5,6) using a 3-to-8 decoder.	KL3
9	Design a code converter for conversion of gray to BCD code.	KL2
10	convert boolean expression in sop. Y(A,B,C) = AB+$\overline{A}$C+BC	KL3
11	Solve the following using Quin-McClusky reduction method f (A, B, C, D) = ∏ M (0,1,2,4,5,6,15)	KL3
12	Implement the following function using 8:1 MUX – $f(A,B,C,D) = \sum m(0,1,2,3,4,9,13,14,15)$	KL3

Unit -3

Short Questions

S. No.	Questions	Bloom Taxonomy
1	Draw only logic diagram of JK Flip-flop.	KL2
2	Draw the excitation table for D flip-flop.	KL2
3	Differentiate between T and D flip flop	KL2
4	Explain Race around condition in a flip flop.	KL1
5	Explain modulus counter using state diagram.	KL1
6	Describe the importance of clock signal in a flip-flop.	KL2
7	Convert JK flip-flop to T flip-flop	KL3
8	difference between JK and SR flip flop.	KL2

Long Questions

S. No.	Questions	Bloom Taxonomy
1	Draw the configuration for SIPO register.	KL2
2	Explain the bidirectional shift register along with a diagram.	KL2
3	Explain the 4-bit Johnson ring counter along with circuit diagram and truth table.	KL2
4	Design a Mod 13 down counter.	KL3
5	Design a 4-bit asynchronous up-down counter.	KL3
6	Explain 4-bit SISO shift register.	KL3
7	Convert the RS flip-flop to J K flip-flop and T flip flop.	KL2
8	Explain 3-bit asynchronous counter with diagram and also draw timing diagram.	KL2
9	Explain universal resistor with suitable diagram.	KL2
10	Explain three-bit synchronous counter with diagram and also draw timing diagram.	KL2
11	Explain clocked RS flip flop with operation.	KL2
12	Explain ripple counter with suitable diagram.	KL2
13	Design a 3 bit up-down counter using T flip flop.	KL3
14	Descibe ring counter. How it is differ from the johnson counter?	KL2

Unit -4

Short Questions

S. No.	Questions	Bloom Taxonomy
1	Describe the process of quantization and encoding in Analog-to-Digital converters.	KL2
2	Define quantization for A/D converter.	KL1
3	Describe disadvantages of weighted resistor DAC?	KL2
4	Write two important specifications of D/A converters.	KL2
5	Explain the function of a sample and hold circuit in D/A conversion.	KL2
6	Write two key specifications of A/D converters.	KL2

Long Questions

S. No.	Questions	Bloom Taxonomy
1	Explain the operation of successive approximation ADC with suitable diagram.	KL2
2	Explain 3-bit flash type or parallel comparator ADC with suitable diagram with truth table. Also give its	KL2
3	Explain the dual slope ADC,comparator with suitable diagram and define various characteristics of ADC.	KL2
4	Explain 3 bit weighted resister type DAC,Comparatorwith suitable diagram. And give its advantages and	KL2
5	Explain 3 bit R-2R ladder r type DAC,converter with suitable diagram. And give its advantages and	KL2
6	Define resolution,conversion time,sensitivity and accuracy of A/D converter.	KL2
7	Explain the imporatant specifications of DAC.	KL2

Unit -5

Short Questions

S. No.	Questions	Bloom Taxonomy
1	Draw block diagram of PLA.	KL2
2	Explain purpose of using PLD	KL2
3	Define sequential memory.	KL1
4	Define volatile and Non-Volatile memory	KL1
5	Discuss about utility of PLDs and state its advantages	KL2
6	Describe sequential memory with an example.	KL2
7	Define Programmable Logic Array (PLA).	KL1

Long Questions

S. No.	Questions	Bloom Taxonomy
1	Explain PLA and give advantages of PLDs.	KL2
2	Differentiate between CPLD and FPGA.	KL2
3	Describe the programmable read-only memor. How it differs from RAM?	KL2
4	Discuss the working of dynamic RAM. Alos explain MROM,PROM,EPROM,EEPROM.	KL2
5	Describe the working principle and applications of Content Addressable Memory (CAM).	KL2
6	Describe the structure and operation of a Programmable Logic Array (PLA).	KL2
7	Compare Programmable Array Logic (PAL) and Complex Programmable Logic Devices (CPLDs).	KL4