Satyug Darshan Institute of Technology,Faridabad

Programme: BCA-DS	**Year:1st Semester:1 st sem**
Subject Name : Computer Organisation	**Subject Code:BCG-105-V1**
Department of Computer Science and Engg.	**AY: 2025-202**
Prepared By: Ms. Mrinal Manjari	

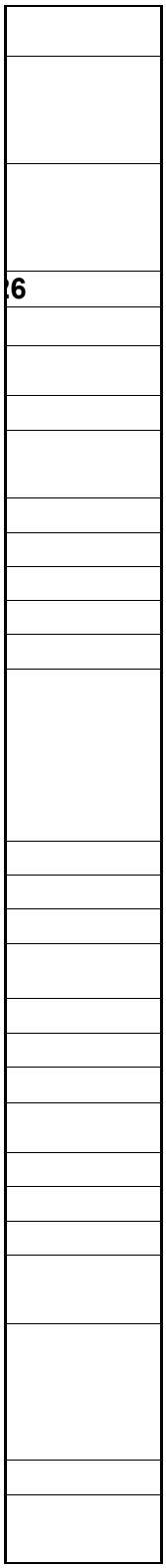
Unit -1

Short Questions

S. No.	Questions	Bloom Taxonomy
1	Define Logic Gates.	KL1
2	Differentiate between POS and SOP form.	KL1
3	Define Parity bit.	KL2
4	Perform the addition : (235)16+(563)8	KL1
5	Convert into gray code for (100100011)2	KL1
6	Convert the following– (i) (34.25)10 =(---)2,(ii) 4F+2D ,(iii)(1101)2*(101)2,(iv) (35)8-(26)8 (v) (7A3F)16 =(……)2=(……)8= (……)10	KL2
7	Simplify using Boolean laws: A+A'B	KL2
8	Explain min-terms and max-terms with the help of a suitable example.	KL1
9	Define cell, pair, quad and octet in K-map.	KL1
10	Given the reason why we are using K-map and Boolean laws in designing the digital circuit.	KL1
11	Design XOR gate using only NOR gates.	KL2
12	Convert the binary code (1001101)2 to Gray Code.	KL2
13	Write the excess-3 code of (124).	KL2
14	Explain self-complementing codes.	KL2
15	Given the data word 01011011 generate the Hamming code for error detection and correcti	KL2
16	State and proved Demorgan's Theorem.	KL2

Long Questions

1	Define Von Neumann Architecture. Explain its major components with a diagram.	KL2
2	Solve the following: (i) (34)10–(56)10 using 2s complement method. (ii) (12)8*(25)8	KL2
3	Define universal gates. Explain why these gates are called universal gates.	KL2
4	Explain Hamming code.Encode a binary word 11001 into the even parity hamming code.	KL2


26

5	Differentiate between SOP and POS forms with suitable examples.	KL2
6	Define Boolean Algebra. State its basic laws and theorems.	KL2
7	Simplify the following function into minimal form using K-Maps and design the circuit (, , ,)=∑ (0,1,2,5,8,9,10)	KL3
8	Implement the following Boolean function with NAND gates. $f(A,B,C)=\sum m(1,2,3,4,5,7)$	KL3
9	Write -28 and +28 in Sign-magnitude representation, 1's Complement representation and 2's Complement representation.	KL3
10	Perform the following using 1's C and 2's C : (i) -89+32 (ii) -23-46	KL3
11	Differentiate between combinational and sequential circuits.	KL3
12	Simplify using K map and implement using only NAND gates:F(A, B, C, D)= Π M (0, 1, 2, 3	KL3
13	What are the error detection and correction codes? How these are helpful in error detection and correction explain with the help of an example.	KL3
14	"Implement the following function using Boolean algebra F(A, B, C, D) = Σm(2,3,4,6,7) ."	KL3

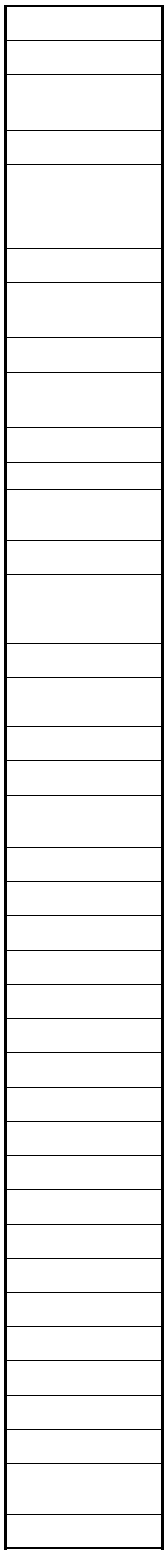
Unit -2

Short Questions

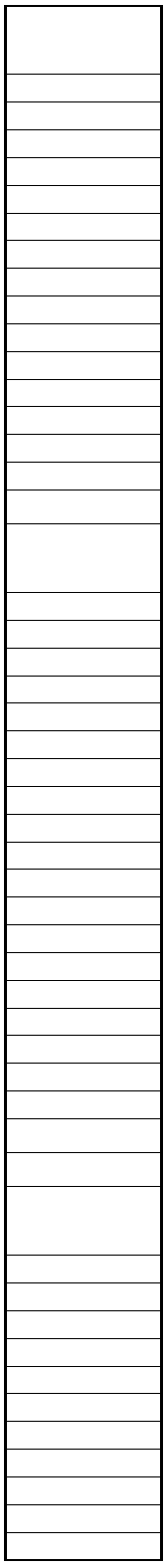
S. No.	Questions	Bloom Taxonomy
1	Differentiate between JK and SR flip-Flop.	KL1
2	Define flip-flop.How it is different from latch.	KL2
3	Discuss briefly 4:1 Multiplexer.	KL1
4	Write the application of shift register.	KL2
5	How can a DEMUX be used as a decoder?	KL1
6	Discuss briefly 1:4 Demultiplexer.	KL2
7	Give some of the major applications of multiplexers.	KL2
8	Realize AND and OR function using 2:1 MUX.	KL2
9	Implement the following function using Boolean algebra F(A, B, C, D) = Σm(2,3,4,6,7) .	KL3
10	Explain 3-to 8-line decoder.	KL2
	Long Questions	
1	Explain one bit memory cell.Make T flip-flop using D-flip-flop	KL2
2	Define decoder.Draw and explain the operation of 2-to-4 line decoder.	KL2
3	Define Multiplexer.Implement 16:1 MUX with 8:1 MUX.	KL4
9	Differentiate between combinational and Sequential circuit.Explain operation of JK flip-flop.	KL3
10	Draw and explain the diagram of parallel input serial out shift register	KL3
11	Explain a 4-bit register with parallel load using block diagram.	KL3
12	Explain half adder and full adder with truth table and logic diagram.	KL3
1	Explain binary half and Full adder subtractor with logic diagram.	KL3
14	Explain bidirectional shift register with parallel load.	KL3
15	Compare synchronous and asynchronous counters.	KL3
16	Explain 4-bit asynchronous (ripple) binary counter with timing diagram.	
17	Explain 4-bit synchronous (ripple) binary counter with timing diagram.	

Unit -3

Short Questions



S. No.	Questions	Bloom Taxonomy
1	Define an instruction code.	KL1
2	Explain the role of computer registers.	KL2
3	List different types of computer instructions.	KL1
4	What is meant by timing and control in a computer?	KL2
5	Define instruction cycle.	KL1
6	Explain memory-reference instructions.	KL2
7	What is an interrupt?	KL1
8	State the purpose of input–output interrupt.	KL2
9	Define accumulator.	KL1
10	Explain stack organization.	KL2
11	What is an instruction format?	KL1
12	List any two addressing modes.	KL1
13	Explain RISC architecture.	KL2
14	Write one difference between RISC and CISC.	KL2
15	What are program control instructions?	KL2
	Long Questions	
S. No.	**Questions**	**Bloom Taxonomy**
1	Explain instruction codes and computer registers with suitable examples.	KL2
2	Describe different types of computer instructions.	KL2
3	Explain the timing and control unit of a basic computer with diagram.	KL3
4	Explain the instruction cycle with a neat diagram.	KL2
5	Discuss memory-reference instructions in detail.	KL3
6	Explain input–output interrupts and their working.	KL2
7	Describe the complete computer system with block diagram.	KL3
8	Explain the design of a basic computer.	KL3
9	Explain the design and working of accumulator logic.	KL3
10	Describe general register organization of CPU.	KL2
11	Explain stack organization and its operations.	KL3
12	Explain instruction formats with suitable examples.	KL2
13	Explain different addressing modes with examples.	KL3
14	Discuss data transfer and manipulation instructions.	KL3
15	Explain program control instructions in detail.	KL3
16	Explain RISC architecture and its advantages.	KL2
17	Compare RISC and CISC architectures.	KL4
18	Given the following information:Program Counter (PC) = 300Index Register (XR) = 40Base	KL3
19	Given:PC = 400Index Register (XR) = 60Base Register (BR) = 500Address field = 120Mem	KL3
	UNIT-4	
	Short Questions	
S. No.	**Questions**	**Bloom Taxonomy**
1	Define parallel processing.	KL1
2	What is pipelining in computer architecture?	KL2
3	Define arithmetic pipeline.	KL1
4	What is an instruction pipeline?	KL2
5	What is RISC pipeline?	KL2
6	Define peripheral devices.	KL1
7	What is an input–output interface?	KL1
8	What is asynchronous data transfer?	KL2
9	List different modes of data transfer.	KL1
10	What is a priority interrupt?	KL2
11	Define Direct Memory Access (DMA).	KL1



12	What is an Input–Output Processor (IOP)?	KL1
13	Define memory hierarchy.	KL1
14	What is main memory?	KL1
15	What is auxiliary memory?	KL1
16	Define associative memory.	KL2
17	What is cache memory?	KL1
18	Define virtual memory.	KL2
19	What is memory management hardware?	KL1

Long Questions

S. No.	Question	Bloom Taxonomy
1	Explain parallel processing and its advantages.	KL2
2	Explain the concept of pipelining with suitable examples.	KL3
3	Describe the working of an arithmetic pipeline with diagram.	KL3
4	Explain instruction pipeline and its hazards.	KL3
5	Explain the working of RISC pipeline.	KL2
6	Explain different types of peripheral devices.	KL2
7	Describe input–output interface in detail.	KL2
8	Explain asynchronous data transfer with handshaking.	KL3
9	Discuss various modes of data transfer.	KL2
10	Explain priority interrupt with suitable diagram.	KL3
11	Describe Direct Memory Access (DMA) and its working.	KL3
12	Explain the role of Input–Output Processor (IOP).	KL2
13	Explain memory hierarchy and its characteristics.	KL2
14	Describe main memory organization.	KL2
15	Explain auxiliary memory and its types.	KL2
16	Explain associative memory with suitable example.	KL3
17	Explain cache memory organization and mapping techniques.	KL3
18	Explain virtual memory and address translation.	KL3
19	Describe memory management hardware in detail.	KL3
20	A pipeline has 5 stages, each taking 20 ns.Calculate:(a) Time to execute 1 instruction(b)Tim	KL3
21	A processor uses a 5-stage instruction pipeline, where each stage takes 10 ns. The processor executes 20 instructions. Calculate: (a)Total execution time using pipelining (b)Speedup compared to non-pipelined execution (c)Throughput of the pipeline (d)Pipeline efficiency	KL3