

Satyug Darshan Institute of Engineering & Technology, Faridabad

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Unit -1

Short Questions

S. No.	Question	KL
1	Define CPU.	KL1
2	List the major components of a computer system.	KL1
3	Explain the function of the memory subsystem.	KL2
4	State the role of the input-output subsystem.	KL2
5	Define the control unit.	KL1
6	Explain the working of the control unit.	KL2
7	Define Instruction Set Architecture (ISA).	KL1
8	List different types of CPU registers.	KL1
9	Explain the role of registers in instruction execution.	KL2
10	List the steps involved in the instruction execution cycle.	KL1
11	Explain RTL (Register Transfer Language).	KL2
12	Define addressing mode.	KL1
13	List any two addressing modes.	KL1
14	Explain the significance of an instruction set.	KL2
15	Name any two common CPUs and their architectures.	KL1

Long Questions

S. No.	Question	KL
1	Explain the CPU, memory, input-output subsystems, and control unit with the help of neat block diagrams.	KL2
2	Discuss the Instruction Set Architecture of a CPU, explaining registers and instruction formats.	KL2
3	Explain the instruction execution cycle with suitable diagrams and	KL2
4	Describe RTL interpretation of instructions with examples.	KL3
5	Discuss various addressing modes used in CPUs with suitable	KL3
6	Explain the structure and importance of an instruction set in CPU	KL2
7	Evaluate how ISA design affects CPU performance, power consumption, and scalability.	KL4
8	An instruction has an address field value 500. The memory contents are $M[500] = 1200$ and $M[1200] = 3500$. Determine the effective address using Direct and Indirect Addressing Modes.	KL3
9	An instruction contains an address field value 400 and the Index Register contains 80. Determine the effective address using Indexed Addressing Mode.	KL3
10	An instruction has an address field value 200 and the Program Counter (PC) value is 1200. Determine the effective address using Relative Addressing Mode.	KL3
11	Explain signed number representation methods with suitable examples.	KL4
12	Discuss fixed-point and floating-point number representations and compare their advantages and limitations.	KL2
13	Explain character representation schemes used in computers.	KL2

14	Explain integer addition and subtraction using 2's complement representation with examples.	KL2
15	Describe the working of a ripple carry adder and carry look-ahead adder with neat diagrams.	KL2
16	Explain binary multiplication using shift-and-add and Booth's	KL2
17	Discuss carry save multiplication and explain how it improves multiplication speed.	KL3
18	Explain restoring and non-restoring division techniques with examples.	KL2
19	Evaluate the importance of floating-point arithmetic in scientific and real-time applications.	KL4
20	Represent the decimal number -25 using 8-bit 2's complement representation.	KL3
21	Convert the decimal number +19 into 8-bit signed magnitude and 1's complement form.	KL3
22	Represent the decimal number 45.625 in binary fixed-point	KL3
23	Represent the decimal number -13.75 using IEEE-754 single precision floating-point format.	KL4
24	Perform binary addition of 101101 + 011011 using 2's complement method and indicate overflow, if any.	KL3
25	Add two 8-bit binary numbers 11011010 and 10101101 using a ripple carry adder.	KL3
26	Explain the addition of 101011 + 110101 using a carry look-ahead	KL3
27	Multiply 1011×1101 using the shift-and-add multiplication technique.	KL3
28	Perform multiplication of -7×5 using Booth's multiplication	KL3
29	Multiply two binary numbers 1101×1011 using carry save	KL3
30	Divide $101101 \div 0011$ using the restoring division method.	KL3
31	Divide $110010 \div 0101$ using the non-restoring division method.	KL3
32	Perform floating-point addition of $(1.101 \times 2^3) + (1.011 \times 2^2)$.	KL3

Unit -2

Short Questions

S. No.	Question	KL
1	Define control unit.	KL1
2	Define hardwired control unit.	KL1
3	Define microprogrammed control unit.	KL1
4	Define microinstruction.	KL1
5	Define semiconductor memory.	KL1
6	Define Direct Memory Access (DMA).	KL1
7	Expand SCSI.	KL1
8	Explain the function of the control unit.	KL2
9	Explain the working of a microprogrammed control unit.	KL2
10	Explain program-controlled and interrupt-driven I/O.	KL2
11	Explain the difference between privileged and non-privileged	KL2
12	Explain the organization of an I/O subsystem.	KL2
13	List any two advantages of DMA.	KL1
14	Illustrate the working of DMA with a suitable diagram.	KL3
15	Illustrate the interaction between a process and the I/O subsystem.	KL3
16	Explain the 8086 microprocessor with neat diagram	KL2

Long Questions

S. No.	Question	KL
1	Explain the hardwired control unit design approach with a neat	KL2
2	Explain the microprogrammed control unit design approach.	KL2
3	Compare hardwired and microprogrammed control units.	KL4
4	Design a simple hypothetical CPU and explain its control unit	KL4

5	Explain different semiconductor memory technologies.	KL2
6	Explain memory organization in a computer system.	KL2
7	Compare SRAM and DRAM memories.	KL4
8	Explain the input–output subsystem with a neat block diagram.	KL2
9	Explain program-controlled I/O, interrupt-driven I/O and DMA.	KL2
10	Compare program-controlled I/O, interrupt-driven I/O and DMA.	KL4
11	Explain privileged and non-privileged instructions.	KL2
12	Explain software interrupts and exceptions.	KL2
13	Describe the role of interrupts in process state transitions.	KL4
14	Explain SCSI interface in detail.	KL2
15	Explain USB architecture and operation.	KL2
16	Compare SCSI and USB interfaces.	KL4
17	A computer system has 16 address lines and 8 data lines. Calculate (a) the total memory size and (b) the number of memory locations.	KL3
18	Design a memory unit of $4K \times 8$ using $1K \times 4$ memory chips. Determine (a) the number of memory chips required and (b) the number of chips per row.	KL3
19	A memory system has an access time of 80 ns and a cycle time of 120 ns. Determine the maximum memory transfer rate.	KL3
20	An SRAM has an access time of 10 ns and a DRAM has an access time of 60 ns. Calculate how many times SRAM is faster than DRAM.	KL3
21	A CPU executes each instruction in 2 μ s. If 5000 instructions are required to transfer one data block using program-controlled I/O, calculate the total transfer time.	KL3
22	In an interrupt-driven I/O system, the interrupt service time is 20 μ s and the interrupt rate is 200 interrupts per second. Calculate the CPU time spent handling interrupts per second.	KL3
23	A DMA controller transfers 4 bytes per cycle with a bus clock frequency of 10 MHz. Calculate the DMA data transfer rate in MB/s.	KL3
24	An interrupt system has an instruction completion time of 3 μ s, interrupt recognition time of 2 μ s, and context saving time of 5 μ s. Find the total interrupt response time.	KL3
25	A USB interface operates at 480 Mbps with 80% efficiency. Calculate the effective data transfer rate.	KL3
26	A SCSI bus transfers 16 bits per cycle at a clock speed of 40 MHz. Calculate the maximum throughput in MB/s.	KL3

Unit -3

Short Questions

S. No.	Question	KL
1	State the basic concept of pipelining.	KL1
2	State the meaning of pipeline throughput.	KL1
3	State the significance of pipeline speedup.	KL1
4	List the types of pipeline hazards.	KL1
5	Identify structural hazards in pipelined processors.	KL1
6	Identify data hazards in pipelined processors.	KL1
7	Identify control hazards in pipelined processors.	KL1
8	State the concept of a parallel processor.	KL1
9	State the need for parallel processors.	KL1
10	State the meaning of concurrent access to memory.	KL1
11	State the purpose of cache coherency.	KL1

Long Questions

S. No.	Question	KL
1	Describe the basic concepts of pipelining.	KL2

2	Illustrate throughput and speedup in pipelined processors.	KL2
3	Describe the organization of parallel processors.	KL2
4	Analyze different types of pipeline hazards and their solutions.	KL3
5	A pipelined processor has 5 stages, each taking 20 ns. Compute the throughput and speedup over a non-pipelined processor.	KL3
6	An instruction pipeline executes 100 instructions with a clock cycle of 10 ns and 4 pipeline stages. Determine the total execution time.	KL3
7	A multiprocessor system has 4 processors sharing a common memory with 20 ns access time. Calculate the effective memory access time assuming simultaneous access without contention.	KL3

Unit -4

Short Questions

S. No.	Question	KL
1	Outline memory interleaving.	KL1
2	Outline hierarchical memory organization.	KL1
3	State the role of cache memory.	KL1
4	Identify cache mapping functions.	KL1
5	List cache mapping techniques.	KL1
6	State the purpose of cache replacement algorithms.	KL1
7	Mention the write-through policy.	KL1
8	Mention the write-back policy.	KL1

Long Questions

S. No.	Question	KL
1	Explain the different cache mapping techniques.	KL2
2	Illustrate memory interleaving with suitable examples.	KL3
3	Examine cache coherency issues in multiprocessor systems.	KL4
4	Analyze the effect of cache size versus block size on performance.	KL4
5	Compare different cache replacement algorithms.	KL4
6	A cache system has a hit ratio of 0.9, cache access time of 10 ns, and main memory access time of 100 ns. Compute the average memory	KL3
7	A direct-mapped cache has 16 cache lines and a block size of 4 words. Determine the number of bits required for the cache line index.	KL3
8	A memory system uses 4-way interleaving with a memory cycle time of 200 ns. Determine the effective memory access time.	KL3
9	A cache memory uses LRU replacement with 4 blocks per set. Calculate the number of bits required to implement the LRU policy.	KL3