Satyug Darshan Institute of Engineering and Technology

Lesson Plan / Teaching Plan / Lecture Plan with Progress : BCA(General+DS) – 1st Semester : 2025-26

Course Name (Code) :Computer Architecture (BCG-105-V1) Faculty – Ms. Mrinal Manjari

Topics / lectures are arranged in sequence - same - as to be taught in the class. Maintain data related to "Date" in its hard copy.

S. No.	Lecture No	Topic Description	Teaching Pedagogy	Reference Material
1	1	UNIT- I Digital Principles: Definition for Digital signals, Digital logic, Digital computers,	Board	T1
2	2	Von Neumann Architecture, Boolean Laws and Theorems	Board	T1
3	3	, K-Map: Truth Tables to K-Map,	Board	T1
4	4	2, 3 and 4 variable K Map, K-Map Simplifications, Don't Care Conditions,	Board	T1
5	5	SOP and POS..	Board	T1
6	6	Number Systems: Decimal, Binary, Octal, Hexadecimal,	Board	T1
7	7	Number System Conversions	Board	T1
8	8	Binary Arithmetic, Addition and subtraction of BCD, Octal Arithmetic, Hexadecimal Arithmetic,	Board	T1
9	9	Binary Codes, Decimal Codes,	Board	T1
10	10	Error detecting and correcting codes,	Board	T1
11	11	ASCII, EBCDIC	Board + PPT	T1
12	12	Excess- 3 Code, The Gray Code	Board + PPT	T1
13	13	Revision	Board + PPT	
14	14	Test		
15	15	UNIT 2 Combinational Circuits: Half Adder and Full Adder,	Board + PPT	T1
16	16	Subtractor, ,	Board	T1
17	17	Decoders, Encoder	Board + PPT	T1
18	18	Multiplexer, Demultiplexer	Board	T1
19	19	Sequential Circuits: Flip-Flops- SR Flip- Flop, D Flip-Flop,	Board	T1
20	20	J-K Flip-Flop, T Flip-Flop.	Board	T1
21	21	Register: 4 bit register with parallel load,	Board + PPT	T1
22	22	Shift Registers- Bidirectional shift register with parallel load	Board	T1
23	23	Binary Counters-4 bit synchronous and	Board	T1
24	24	Asynchronous binary counter.	Board	T1
25	25	Revision	Board + PPT	
26	26	Test	Board	
27	27	UNIT-III Basic Computer Organization and Design: Instruction Codes,	Board + PPT	T1,T2
28	28	Computer Registers, Computer Instructions,	Board	T1,T2
29	29	Timing and Control, Instruction Cycle,	Board	T1,T2
30	30	Memory-Reference Instructions, Input- Output Interrupt, Complete Computer Description,	Board	T1,T2
31	31	Design of Basic Computer, Design of Accumulator logic.	Board	T1,T2
32	32	Central Processing Unit: Introduction, General Register Organization,	Board	T1,T2
33	33	Stack Organization,	Board	T1,T2
34	34	Instruction Formats, Data Transfer and Manipulation	Board + PPT	T1,T2
35	35	Addressing Modes,	Board	T1,T2
36	36	Program Control, Reduced Instruction Set Computer(RISC), RISC Vs CISC.	Board	T1,T2
37	37	Test	Board	
38	38	Pipeline and Vector Processing: Parallel Processing,	Board	T1,T2
39	39	Pipelining, Arithmetic Pipeline	Board	T1,T2
40	40	Instruction Pipeline, RISC Pipeline	Board + PPT	T1,T2
41	41	Input-Output Organization: Peripheral Devices, Input Output Interface,	Board + PPT	T1,T2
42	42	Asynchronous data transfer, Modes of Transfer,	Board + PPT	T1,T2
43	43	Priority Interrupt,	Board	T1,T2
44	44	Direct memory Access,	Board	T1,T2
45	45	Input-Output Processor(IOP).	Board	T1,T2
46	46	Memory Organization: Memory Hierarchy,.	Board	T1,T2

47	47	Main Memory, Auxiliary memory, Associate Memory,	Board	T1,T2
48	48	Cache Memory,	Board	T1,T2
49	49	Virtual Memory,	Board	T1,T2
50	50	Memory Management Hardware	Board	T1,T2
51	51	Revision	Board + PPT	
52	52	PYQ		

Study Material / Books / Web-resources / Online Courses Links etc.

S. No.	Description
1	Donald P Leach, Albert Paul Malvino, Goutam Saha- "Digital Principles & Applications" , Tata McGraw Hill Education Private Limited,2011Edition. 2
2	. M. Morris Mano- "Computer System Architecture", Pearson/Phi, Third Edition.