Satyug Darshan Institute of Engineering and Technology				
sson Plan / Teaching Plan / Lecture Plan with Progress : BCA-DS Semester 4 th AY: 2025-				
Course Name (Code) :BCG-208-V				
Teacher Centric Approaches => TC-1 (Chalk and Talk); TC-2 (PPT); TC-3 (Video Lectures)Learner (Student) Centric Approaches => LC-1 (Assignment); LC-2 (Mini Project); LC-3 (Quiz); LC-4 (Seminar on recent trends); LC-5 (Group Task); Any other				
Topics / lectures are arranged in sequence - same - as to be taught in the class. Maintain data related to "Date" in its hard copy.				
S. No.	**LecNo**	**Topic Description**	**Teaching Pedagogy**	**Reference Material**
1	1	Introduction		
2	2	CPU	TC-1	R1,R2
3	3	memory, input-output subsystems,	TC-1	R1,R2
4	4	control unit.	TC-1	R1,R2
5	5	Instruction set architecture of a CPU – registers,	TC-1	R1,R2
6	6	instruction execution cycle,	TC-1	R1,R2
7	7	instruction execution cycle,	TC-1,TC2	R1,R2
8	8	RTL interpretation of instructions,	TC-1	R1,R3
9	9	addressing modes,	TC-1,TC2	R1,R2
10	10	instruction set.	TC-1,TC2	R1,R2
11	11	Case study – instruction sets of some common CPUs.	TC-1	R1,R2
12	12	signed number representation,	TC-1	R1,R2
13	13	fixed and floating point representations,	TC-1	R1,R2
14	14	character representation.	TC-1	R1,R2
15	15	Computer arithmetic – integer addition	TC-1,TC2	R1,R2
16	16	Computer arithmetic – subtraction, ripple carry adder,	TC-1,TC2	R1,R2
17	17	carry look-ahead adder, etc.	TC-1	R1,R2
18	18	multiplication – shift-	TC-1,TC2	R1,R2
19	19	multiplication - add,	TC-1,TC2	R1,R2

20	20	multiplication – Booth multiplier,	TC-1,TC2	R1,R2
21	21	multiplication – carry save multiplier, etc.	TC-1,TC2	R1,R2
22	22	Division restoring and non-restoring techniques,	TC-1,TC2	R1,R2
23	23	Division non-restoring techniques,	TC-1,TC2	R1,R2
24	24	floating point arithmetic	TC-1	R1,R2
25	25	"Introduction to x86 architecture:	TC-1,TC2	R1,R2
26	26	CPU control unit design	TC-1	R1,R2
27	27	hardwired and micro-programmed design approaches,	TC-1	R1,R2
28	28	hardwired and micro-programmed design approaches,	TC-1,TC2	R1,R2
29	29	Case study – design of a simple hypothetical CPU."	TC-1	R1,R2
30	30	Memory system design: semiconductor memory technologies, memory organization.	TC-1	R1,R2
31	31	Peripheral devices and their characteristics: Input-output subsystems,	TC-1,TC2	R1,R2
32	32	I/O device interface,	TC-1	R1,R2
33	33	I/O transfers – program controlled,	TC-1,TC2	R1,R2
34	34	interrupt driven and DMA,	TC-1	R1,R2
35	35	privileged and non-privileged instructions,	TC-1	R1,R2
36	36		TC-1	R1,R2
37	37	Programs and processes – role of interrupts in process state transitions,	TC-1	R1,R2
38	38	software interrupts and exceptions.	TC-1	R1,R2

39	39	I/O device interfaces – SCII, USB	TC-1,TC2	R1,R2
40	40	Basic concepts of pipelining,	TC-1	R1,R2
41	41	throughput and speedup,	TC-1	R1,R2
42	42	pipeline hazards.	TC-1	R1,R2
43	43	Parallel Processors: Introduction to parallel processors,	TC-1	R1,R2
44	44	Concurrent access to memory ,cache coherency.	TC-1	R1,R2
45	45	Memory organization: Memory interleaving,	TC-1,TC2	R1,R2
46	46	concept of hierarchical memory organization,	TC-1,TC2	R1,R2
47	47	cache memory, cache size Vs block size,	TC-1,TC2	R1,R2
48	48	mapping functions,	TC-1,TC2	R1,R2
49	49	replacement algorithms,	TC-1	R1,R2
50	50	write policies.	TC-1	R1,R2
REFERENCES				
1. Computer System Architecture by Maris Mano				
2. Computer System Architecture by Rajib Mall				